I claim:

1. An integrated circuit comprising:

a. an intellectual property core free of any boundary scan register; and

b. a test access port formed in the core, the test access port including test port interface signal leads and additional test input, test output and test control signal leads.

2. The integrated circuit of claim 1 in which the additional test signal leads include an external register present signal lead.

3. The integrated circuit of claim 1 including a scan register formed on the integrated circuit outside of the core, the scan register being connected to the test access port through the additional test input, test output and control signal leads.

4. The integrated circuit of claim 3 in which the scan register is a boundary scan register and the additional test signal leads include an external register present lead connected to indicate the presence of the boundary scan register.

5. The integrated circuit of claim 3 in which the scan register is a boundary scan register.

6. The integrated circuit of claim 3 wherein the scan register is a general purpose scan register.

7. The integrated circuit of claim 3 in which the additional test signal leads include an external register present lead connected to indicate the presence of a connected scan register.

8. The integrated circuit of claim 3 including electrically programmable circuits, the scan register being connected to the electrically programmable circuits for programming the electrically programmable circuits.

9. The integrated circuit of claim 1 in which the test access port includes a capture-shift-update register, a decode section and an external register present lead connected to both the capture-shift-update register and the decode section.

10. The integrated circuit of claim 1 in which the test port interface signal leads include a test data input signal lead, a test clock signal lead, a test mode select signal lead, a test reset signal lead and a test data output signal lead and the additional test input, test output and test control signal leads include a serial data output signal lead, a serial data input signal lead, a control signal lead and an external register present signal lead.

11. A process of executing boundary scan instructions at a test access port comprising:

a. sensing that the external register present signal is in a logical condition indicating the absence of a user-added boundary scan register; and

b. causing all boundary scan instructions to default to a bypass instruction.

12. The process of claim 11 in which the causing includes causing at least one of extest, intest, sample/preload, highz and clamp instructions to default to the bypass instruction.

13. A process of determining the presence of a user-added scan register comprising:

a. capturing a logical state of an external register present signal in a shift register;

b. shifting the contents of the shift register out of the shift register; and

c. examining the logical state of the external register present signal in the contents of the shift register shifted out of the shift register.

14. The process of claim 12 including capturing other status signals in the shift register.